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FIG. 1

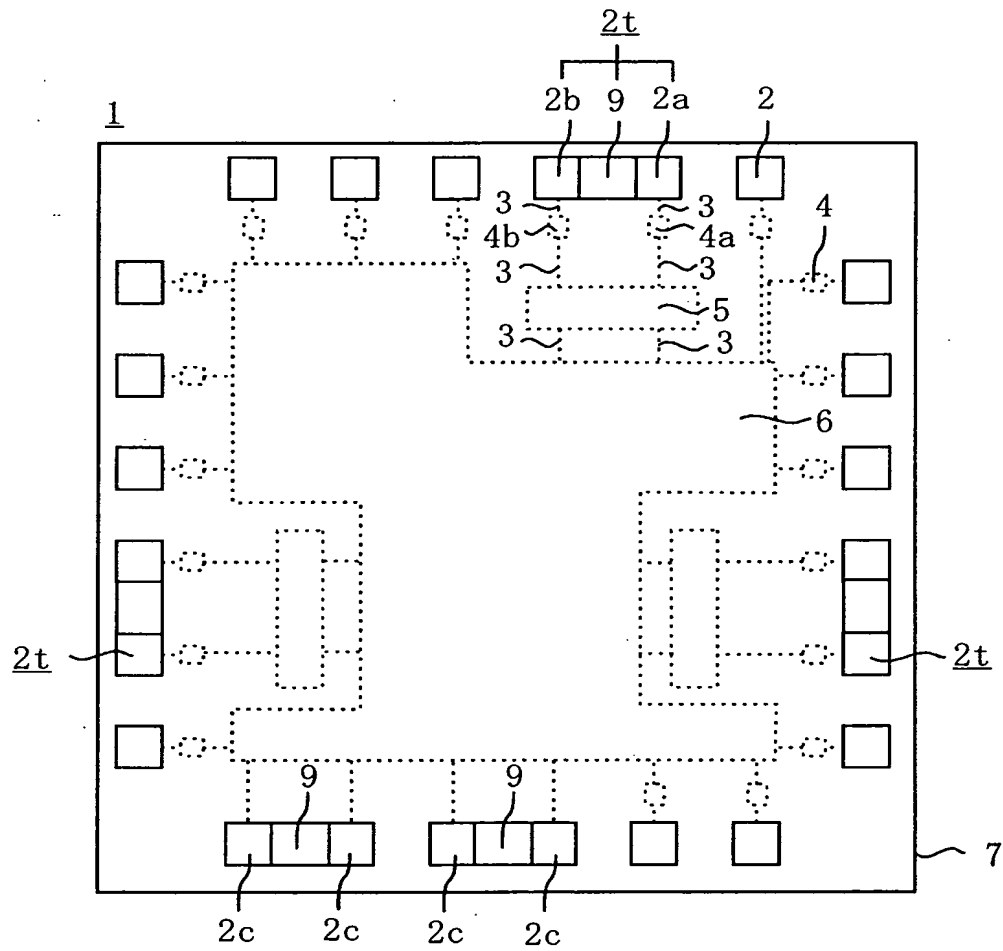


FIG. 2A

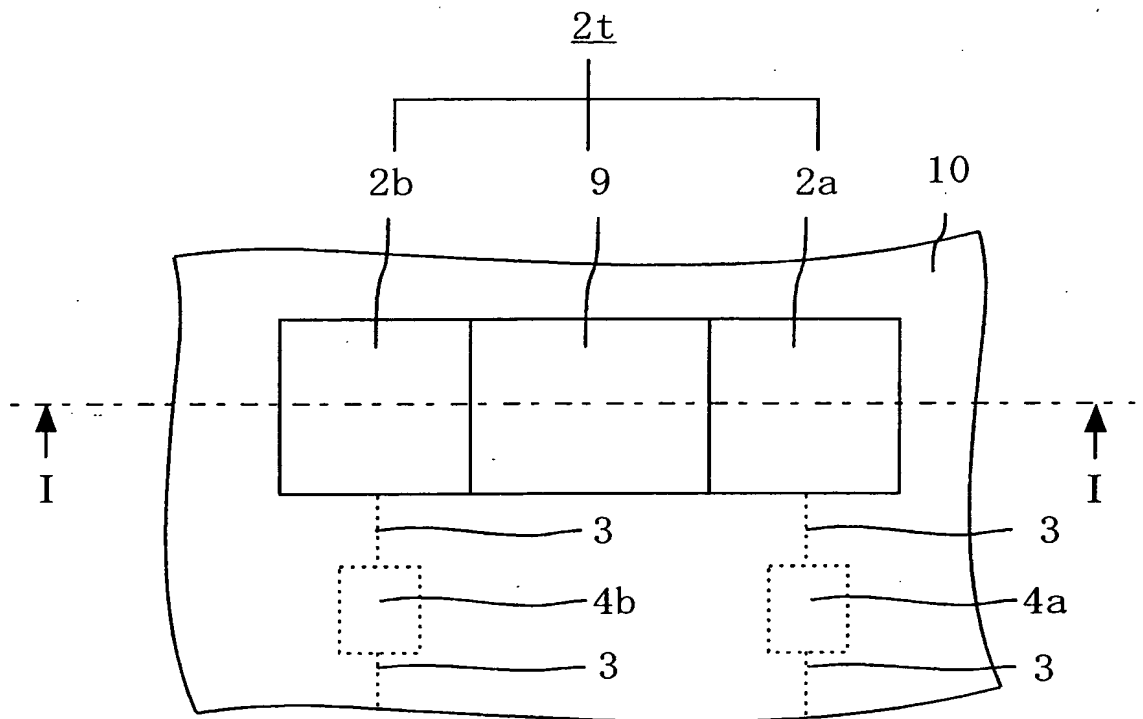


FIG. 2B

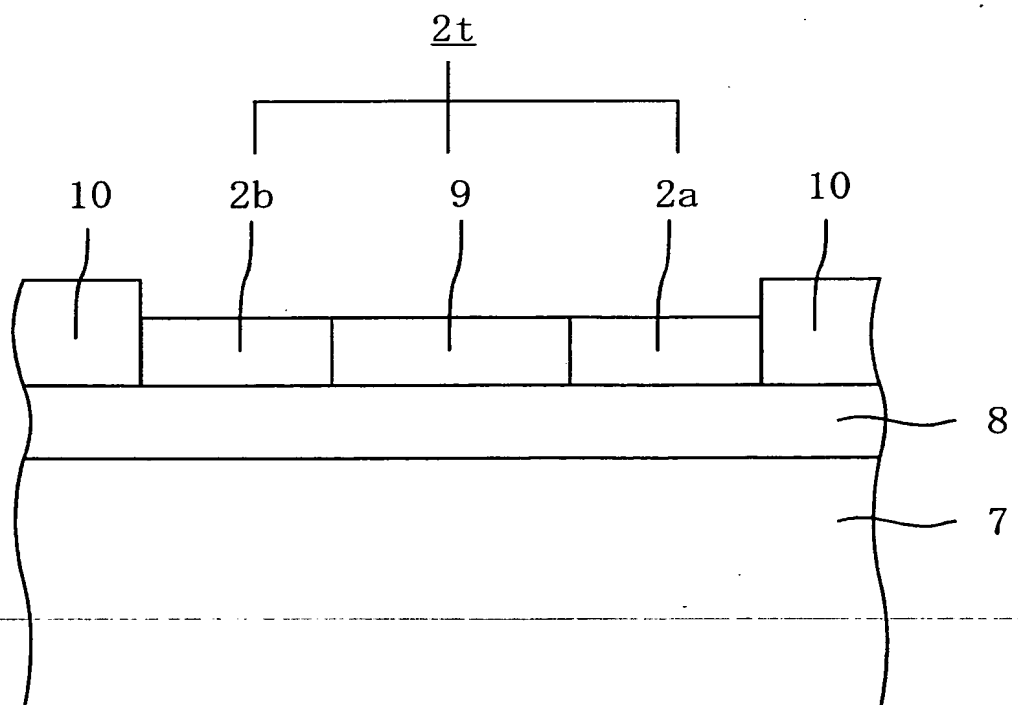


FIG. 3

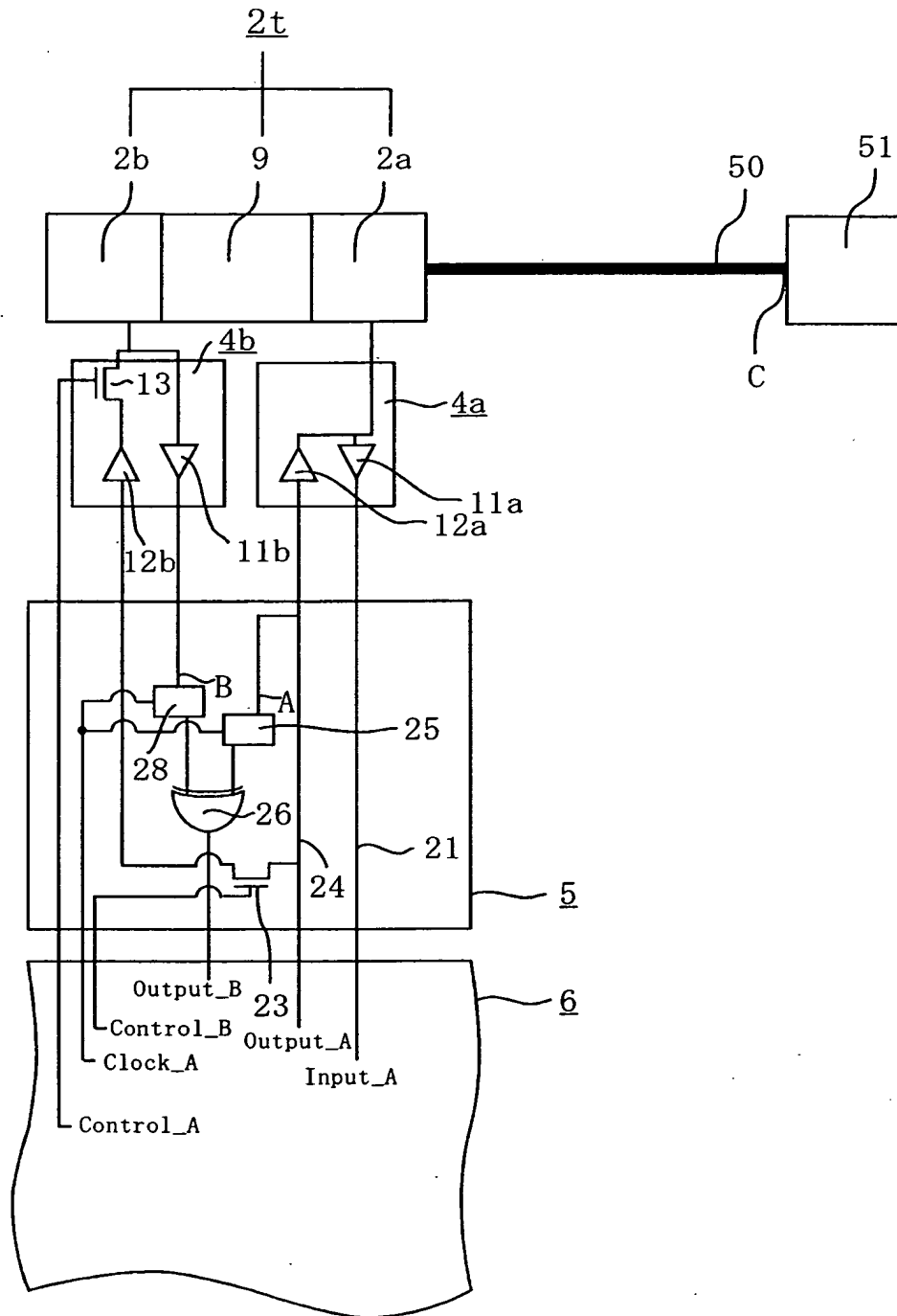


FIG. 4

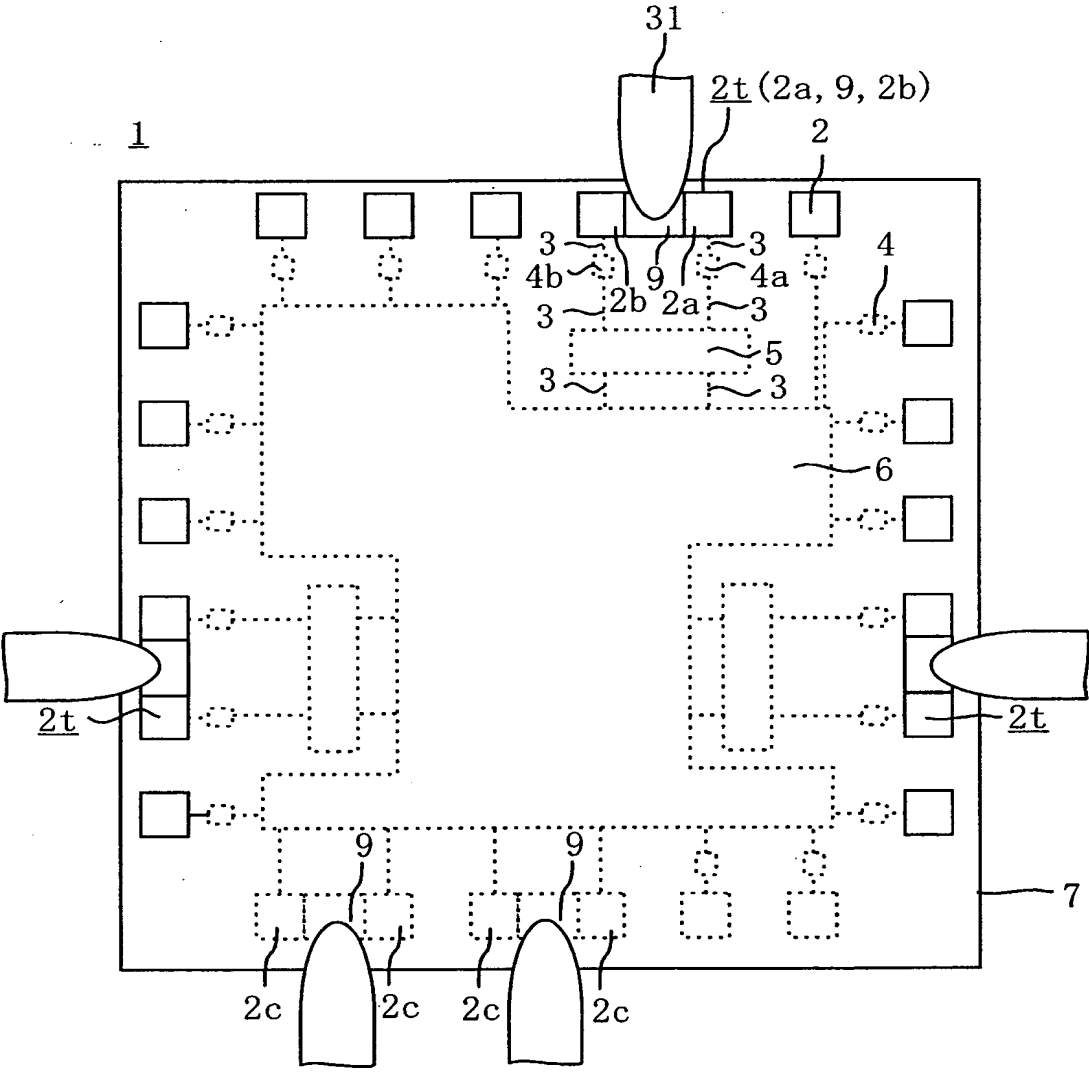


FIG. 5

Operation Mode	Signal pin name	Control_A	Control_B	Clock_A
	Test pad input/output status			
Normal operation mode	Input	0	0	0
	Output	0	0	0
First test mode	Input	0	0	0
	Output	1	1	0
Second test mode	Input	0	0	0
	Output	0	0	1

FIG. 6A

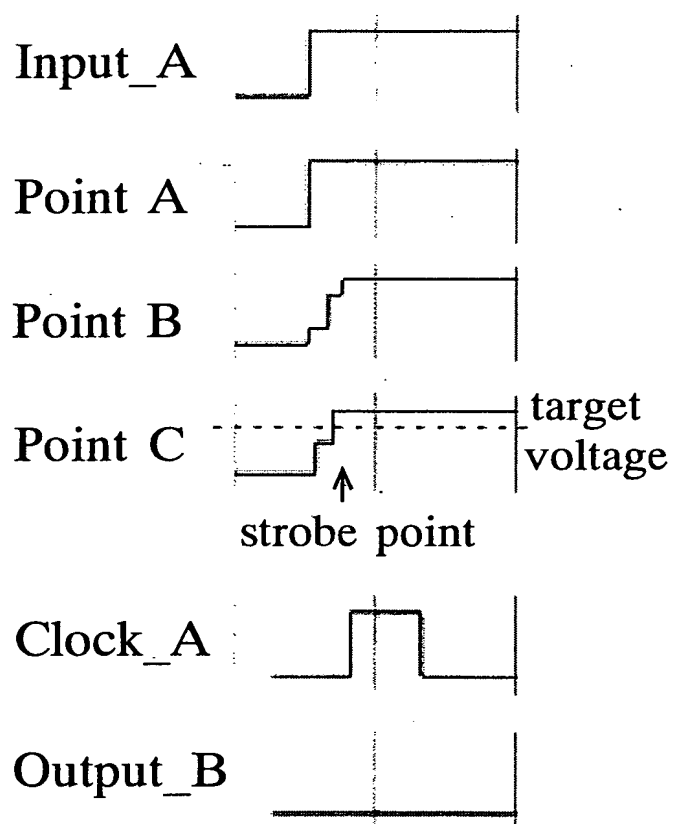


FIG. 6B

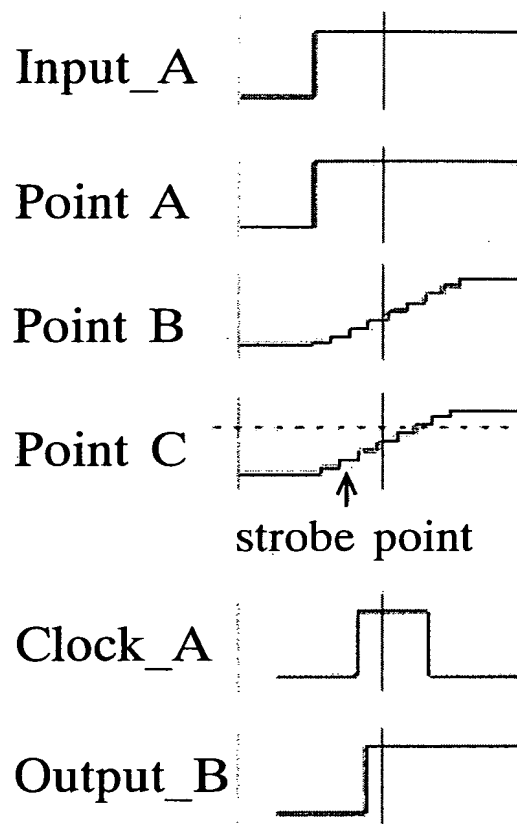


FIG. 7

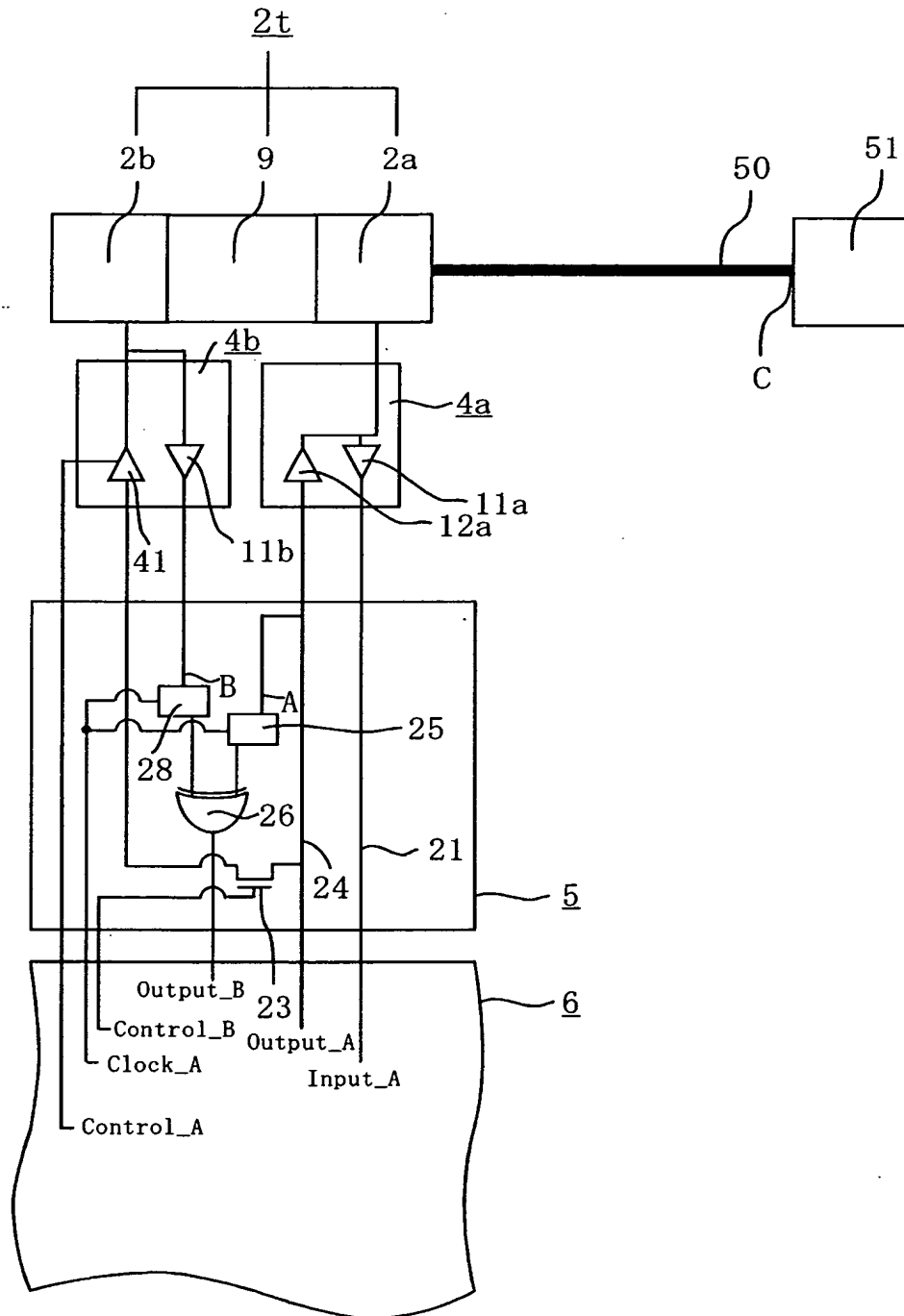




FIG. 8A

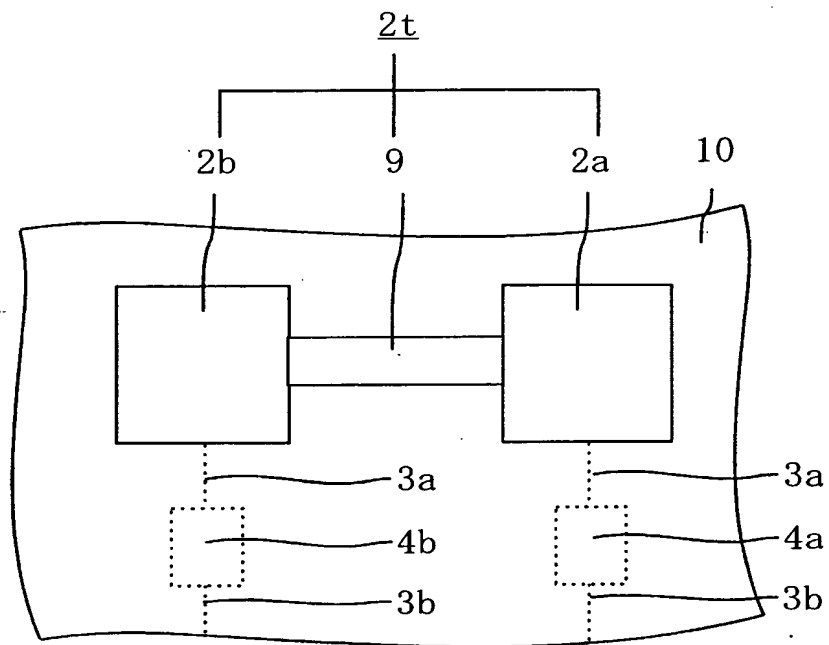


FIG. 8B

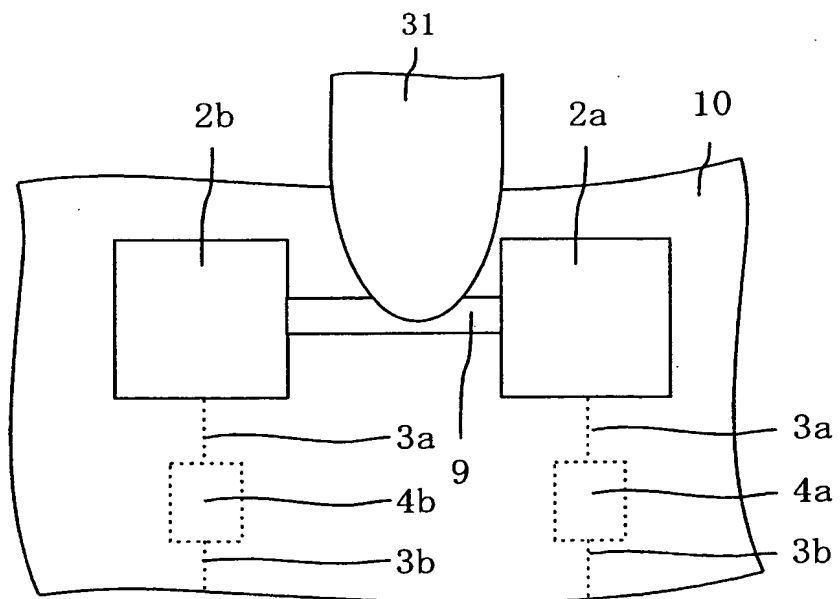


FIG. 9

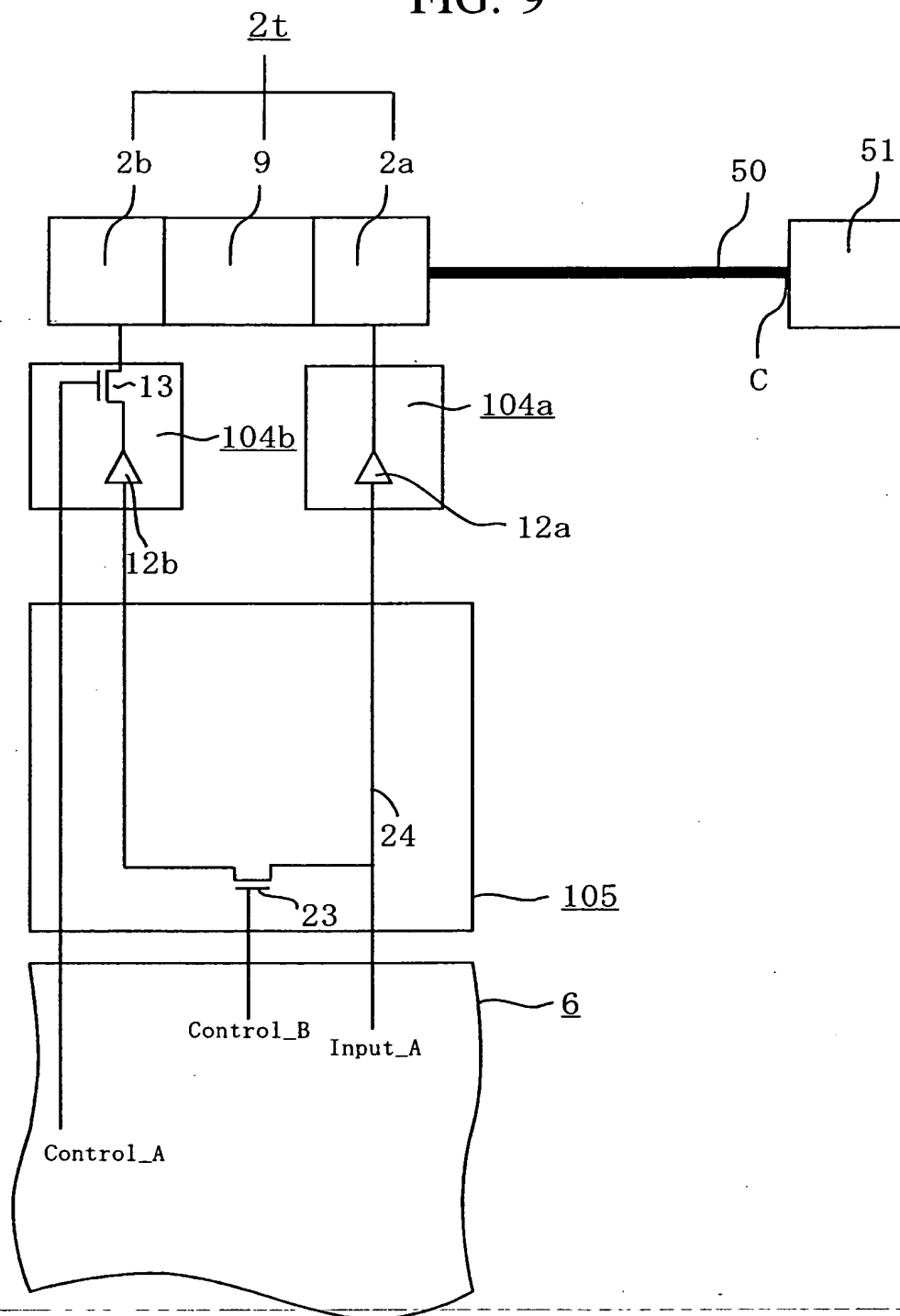


FIG. 10

